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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,308	09/22/2003	Xiangdong Chen	FIS920030266US1	2307

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/605,308	CHEN ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,9,10 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,9,10 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed June 21, 2005 has been entered. Claims 2, 8, and 11-20 have been cancelled. Claims 1, 3, 4, 6, 9 and 10 have been amended. Claims 21-26 have been added. Claims 1, 3-7, 9, 10 and 21-26 are pending.

Allowable Subject Matter

2. The indicated allowability of claims 2, 3 and 10 is withdrawn in view of the newly discovered reference(s) to Lee et al. (U.S. Patent No. 6,331,478). Rejections based on the newly cited reference(s) follow.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested:

CONDUCTOR LINE STACK HAVING THE TOP PORTION OF A SECOND LAYER THAT IS SMALLER THAN THE BOTTOM PORTION.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. . Claims 1, 3-7 and 21-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (U.S. Patent No. 5,331,478).

With respect to claim 1, Lee teaches a conductor line stack as claimed including:

a first layer (12a) consisting essentially of at least one first material layer of a first material selected from the group consisting of polysilicon;

a second layer (17) consisting essentially of at least one second material formed on the first layer (12a), the second layer having an upper portion (17b) and a lower portion (17a); and

a pair of first spacers (60) disposed on sidewalls of the upper portion (17b), the lower portion (17a) having width defined by a combined width of the upper portion (17b) and the pair of first spacers (60). (See Fig. 1E).

Note that, the width of bottom portion (17a) is equal to (or defined by) the width of top portion (17b) plus the portion of material that fill the groove (52).

With respect to claim 21, Lee teaches a conductor line stack as claimed including:

a first layer (12a) consisting essentially of a doped polysilicon;

a second layer (17) disposed on the first layer (12a), the second layer (17) consisting essentially of at least one second material selected from the group consisting of metals and conductive compounds of metals, the second layer (17) having an upper portion (17b) and a lower portion (17a); and

a pair of first spacers (60) disposed on sidewalls of the upper portion (17b), the lower portion having width defined by the width of the upper portion (17b) combined with a width of the pair of spacers (60). (See Fig. 1E).

Regarding the width of the bottom portion of the second layer, the same reasoning as that of claim 1 also applies.

With respect to claim 3, the second material of Lee includes a metal.

With respect to claims 4 and 22, the conductor line stack of Lee further comprises an insulating cap (20) disposed over the second layer (17) and spacers (60) disposed on sidewalls of the lower portion (17a) and on sidewalls of the first layer (12a).

Note that, since the spacers are of the same material, thus it can be seen as one portion that fill the groove and the other portion that cover the remaining sidewalls.

With respect to claims 5 and 23, the conductor contact structure of Lee includes the conductive line stack and further includes a borderless bitline contact (75) to a single-crystal semiconductor region (10) disposed below the conductor line stack, the bitline contact (75) having a sidewall contacting a sidewall of the spacers (60).

With respect to claims 6 and 24, the conductor contact structure of Lee includes a pair of conductive line stack, the conductor line stacks being oriented in parallel, the conductor contact structure of Lee includes a borderless bitline (75) contact to a single-crystal semiconductor

region (10) dispose below the pair of conductor line stacks, the bitline contact (75) contacting sidewalls of the spacers (60) of the conductor line stacks.

With respect to claims 7 and 25, the borderless bidline contact (75) of Lee includes heavily doped polysilicon.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee '478 as applied to claims 6 and 24 above, and further in view of Divakaruni et al. (U.S. Patent No. 6,426,247) of record.

Lee teaches the conductor contact structure includes a pair of conductor line stacks being oriented in parallel, wherein a first conductor line stack of the pair is separated from the single-crystal semiconductor region (10) by an array top oxide layer (11a).

Thus, Lee is shown to teach all the features of the claim with the exception of the second conductor line of the pair is conductively coupled to a gate conductor of a vertical passgate transistor of a DRAM.

However, Divakaruni teaches one of the conductor line stack of the pair is conductively coupled to a gate conductor of a vertical passgate transistor of a DRAM (3). (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the second conductor line stack of Lee conductively coupled to a gate conductor of a vertical passgate transistor of a DRAM as taught by Divakaruni to form an IC circuit since conductor line stacks are known to be used connecting various devices in a circuit including DRAM.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee '478 in view of Divakaruni et al. (U.S. Patent No. 6,426,247) of record.

Lee teaches a conductor contact structure substantially as claimed including:

a pair of conductor line stacks oriented in parallel, each of the conductor line stack includes:

a firs layer (12a) consisting essentially of at least one first material selected from the group consisting essentially of doped polysilicon;

a second layer (17) consisting essentially of at least one material selected from the group consisting of metal and metal silicides overlying the first layer (12a) the second layer (17) having an upper portion (17b) and a lower portion (17a);

an insulating cap (20) formed over the second layer (17); and

a pair of spacers (60) disposed on sidewalls of the upper portion (17b) and the insulating cap (20), the lower portion (17a) having width defined by a combined width of the upper portion (17b) and the spacers; and

the pair of spacers (60) disposed on sidewalls of the lower portion (17a) and on sidewalls of the first layer (12a);

a borderless bitline contact (75) to a single-crystal semiconductor region (10) disposed below the pair of conductor line stacks, the bitline contact contacting sidewalls of the spacers (60) of the conductor line stacks,

wherein a first conductor line stack of the pair of conductor line stacks is separated from the single-crystal semiconductor region by an array top oxide layer (11a). (See Fig. 1H).

Thus, Lee is shown to teach all the features of the claim with the exception of the second conductor line of the pair is conductively coupled to a gate conductor of a vertical passgate transistor of a DRAM.

However, Divakaruni teaches one of the conductor line stack of the pair is conductively coupled to a gate conductor of a vertical passgate transistor of a DRAM (3). (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the second conductor line stack of Lee conductively coupled to a gate conductor of a vertical passgate transistor of a DRAM as taught by Divakaruni to form an IC circuit since conductor line stacks are known to be used connecting various devices in a circuit including DRAM.

Regarding the width of the bottom portion of the second layer, the same reasoning as that of claim 1 also applies.

Regarding the first and second spacers, see claims 4 and 22 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 11, 2005

ANH D. MAI
PRIMARY EXAMINER